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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/688,989	10/17/2000	Yoshitaka TSUNASHIMA	04329.1952-01000	2408

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EXAMINER

RAO, SHRINIVAS H

ART UNIT

PAPER NUMBER

2814

DATE MAILED: 06/06/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/688,989

Applicant(s)

TSUNASHIMA ET AL.

Examiner

Steven H. Rao

Art Unit

2814

-- The MAILING DATE of this communication appears on the cover sheet with the corresponding address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 12 April 2002.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 27, 28 and 30-33 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 27, 28 and 30-33 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 01 October 2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

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***Response to Amendment***

Applicants' amendment filed on March 11, 2002 along with the request for a RCE has been entered on April 12, 2002.

Therefore claims 27,28 31 and 32 as amended by the amendment , claim 33 presently newly added by the amendment and claim 30 as recited in the amendment of June 12, 2001 are currently pending in the application.

***Priority***

Receipt is acknowledged of papers submitted under 35 U.S.C. 120, claiming priority from U.S. Serial No. 09/688989 which papers have been placed of record in the file.

***Continued Prosecution Application***

The request filed on 3/11/2002 for a RCE under 37 CFR 1.17(e) based on parent Application No. 09/688989 is acceptable and a RCE has been established. An action on the RCE follows.

***Preliminary Amendment Status***

Acknowledgment is made of entry of preliminary amendment filed 3/11 /2002 has been entered on April 12, 2002.

***Claim Rejections - 35 USC § 112***

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I. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 27, 28, 30 and 32 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 27 recites a semiconductor device having a semiconductor substrate and a first and second transistors formed thereon and the previously recited insulator films for the transistors have been deleted.

It is not understood how a transistor without an insulating layer between itself and the semi conducting substrate on which it is formed can function as a transistor.

Claims 28, 30 and 32 are rejected at least for depending upon rejected claim 27.

Claim 27 and dependent claims 28,30-33 are also rejected because, claim 27 recites , " a side wall of said first gate electrode at one end of a channel direction is connected to a sidewall of said second gate electrode at one end of the channel direction."

First of all it is not clear what applicants' mean by connected is it electrically connected ?.

Secondly, if the first and second gate electrodes are connected by their sidewalls it is not clear how the device will work.

If applicants' mean by the above recitation, the inter level interconnect that was previously recited in claim 32, then that must be clearly stated.

Appropriate correction is required.

II. Claims 27, 28, 30- 33 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 27 the phrase "a side wall of said first gate electrode at one end of a channel direction is connected to a sidewall of said second gate electrode at one end of the channel direction" renders the claim indefinite because the term "channel direction " is indefinite since the channel has at least four directions and it is not clear which channel direction applicants' are referring to.

Claims 28,30-33 are rejected at least for depending upon rejected claim 27.

In claim 33, the phrase, " said second gate electrode is formed on the poly silicon layer, and said side wall of said first gate electrode is connected to the side wall of said second gate electrode and a side wall of said side insulator film ." It is not understood what applicants' mean by the phrase, "and said side wall of said first gate electrode is connected to the side wall of said second gate electrode and a side wall of said side insulator film."

Appropriate correction is required.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 27, 28, 30-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kume et al. ( U.S. Patent No. 5,188,976, herein after Kume) previously applied and Tada ( U.S. Patent No. 5,497,021, herein after Tada) previously cited but newly applied.

With respect to claim 27, to the extent understood, Kume describes substantially all the structure set forth in the claims except the newly added limitation, " a sidewall of the first gate electrode at one end of a channel direction is connected to a side wall of the second gate electrode at one end of the channel direction '.

However, Tada a patent from the same filed of endeavor, describes in fig. 3(d) and col. 8 lines 1-10 a direct connection between gate electrodes 13 a and b (and also a connection through the interlayer interconnect aluminum layer ) ( i.e. a sidewall of the first gate electrode at one end of a channel direction is connected to a side wall of the second gate electrode at one end of the channel direction) to reduce the device size.

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Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include Tada's direct connection between gate electrodes 13 a and b ( i.e. a sidewall of the first gate electrode at one end of a channel direction is connected to a side wall of the second gate electrode at one end of the channel direction) in Kume's device to reduce the device size (i.e. miniaturization and reducing the chip area of the semiconductor device Tada col. 8 lines 8-11).

With respect to claim 28, wherein a part of the side wall of the first gate electrode is only connected to a part of the sidewall of the second gate electrode and the part of the side wall of the first gate electrode ( Tada fig. 3 d col. 8 lines 1-15, the motivation to combine Kume and Tada given above) and col. and the part of the side wall of the second gate electrode are substantially perpendicular to a surface of the semiconductor substrate . (Kume fig. 18, 35 is perpendicular to 11).

With respect claim 30, to the extent understood, it has not been amended and the previous rejection is maintained.

With respect to claim 31, wherein said first transistor includes a first insulator film and second transistor includes insulator film ( Kume fig. 4 # 18-20,col.8 line 15-first and fig.4 # 27, col. 10 line 55-second ) and the first insulator film is thinner than the second insulator film, the first transistor is included in a logic circuit and the second transistor is included in a memory cell ( Kume figs. 4 and 18).



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With respect to claim 32, to the extent understood, wherein top surfaces of the first and second gate electrodes and a connection layer are coplanar . In addition to the obvious design choice rejection stated in the previous office actions and incorporated here by reference ( see also Tada fig. 3d and col. 8 lines 5-10).

With respect to claim 33, to the extent understood, wherein the device has a gate insulator formed on the substrate ( Kume fig. 4 # 18-20, col. 8 line 15), a poly silicon layer formed on the gate insulator film ( Kume figs. 4 and 18, col. 13 lines 40-45) and a side insulator film formed on a side of the gate insulator film and the poly silicon film ( Kume fig. 18 # 26, col. 8 line 18-19), the second gate electrode is formed on the and the second gate electrode is formed on the poly silicon layer and the side wall of the first gate electrode is connected to the side wall of the second gate electrode and a side wall of the side insulator film.

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Steven H. Rao whose telephone number is (703) 306-5945. The examiner can normally be reached on Monday- Friday from approximately 7:00 a.m. to 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaudhuri Olik can be reached on (703)3062794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 7463926 for regular communications and (703) 872-9319 for After Final communications.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 3067722.



Steven H. Rao

Patent Examiner

June 3, 2002



OLIK CHAUDHURI  
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